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Form PTO 14 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office
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Information Disclosure Statement by Applicant
Applicant: David Muradian et al.
(Use several sheets if necessary) Filed: October 5, 2001 Group: 2858

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
EP	1	5,267,017	11/30/1993	Uritsky et al.	356	375	05/20/1992
EP	2	5,539,752	07/23/1996	Berezin et al.	371	22/1	06/30/1995
EP	3	5,777,901	07/07/1998	Berezin et al.	364	578	09/29/1995
EP	4	5,870,187	02/09/1999	Uritsky et al.	356	237	08/08/1997
EP	5	6,035,244	03/07/2000	Chen et al.	700	110	10/22/1997

Foreign Documents

Init.		Document No.	Date	Country	Class	Subclass	Translation	
							Yes	No
EP	6	EP 0 641 020 A2 & A3	03/01/1995 07/26/1995	Europe	H01L	21/66		

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

EP	7	J. Segal et al, "Determining Redundancy Requirements for Memory Arrays with Critical Area Analysis", Proceedings of the 1999 IEEE International Workshop on Memory Technology, Design, and Testing, IEEE Comput. Soc., August 1999.					
EP	8	J. Segal et al., " A Framework for Extracting Defect Density Information for Yield Modeling from In-line Defect Inspection for Real-time Prediction of Random Defect Limited Yields", Proceedings of the 1999 IEEE International Symposium on Semiconductor Manufacturing, (Piscataway, NJ: Institute of Electrical and Electronics Engineers), pp. 403-406. 1999 (no month)					
EP	9	J. Segal, et al, "Predicting Failing Bitmap Signatures for Memory Arrays with Critical Area Analysis", 1999 Proceedings IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop (ASMC), p. 178-182, 1999.					

Examiner Evan Pert Date Considered 8-18-03

Examiner: Initial if citation considered, whether or not citation is in conference with MPEP 609; Draw line through citation if not conformance and not considered. Include a copy of this form with the next communication to applicant.